ECR #: 47
Title: Timing Margin to Support Spread Spectrum Clocking
Release Date: 8/17/98
Impact: Change
Spec Version: A.G.P. 2.0

Summary:

Systems that use spread spectrum clocking (SSC) must provide at least 0.5 ns of common clock (AGP-1X) timing margin. Add-in cards must produce less than 0.5 ns of common clock timing skew in an SSC system of appropriate modulation levels and rates (see below). All AGP components must be functional with a AGPCLK using SSC.

Background:

Spread spectrum clocking is used as a mechanism to reduce EMI in a system. All system clocks derived from the CPU clock, including the AGPCLK, are FM modulated at a 30 KHz to 50 KHz rate. This spreads the emissions over a wider spectrum and reduces their energy at any single frequency.

SSC causes some timing margin issues when a phased locked loop (PLL) is driven by an AGPCLK with SSC. The PLLs will track the FM modulation with a time lag that is dependent on the loop characteristics of the PLL. This time lag causes a timing skew between the input and output of the PLL. Any circuits that are driven by the PLL outputs will be time skewed with respect to the AGPCLK. Depending on the clocking architecture of the device, this timing skew may show up as timing skew with respect to the AGP-1X timing specifications or may show up as skew across some clock domain boundary internal to the device.

Note that SSC affects only AGP-1X timing parameters. The modulation is slow enough that successive clock period lengths and jitter are not increased. These are the only clock parameters that affect AGP-2X and AGP-4X timings.

The details of SSC theory, impact on PLLs and system timing skew are beyond the scope of this ECR. Two white papers are available to explain SSC and its effects on AGP timing. There is a Mathcad 7 based PLL simulator that can be used to evaluate the timing skew impact of SSC on a particular PLL design. The white papers are titled “SSC-Its Timing Impacts” and “AGP Interface Architectures and Motherboard Design with SSC.”

The SSC papers and simulator are available at *http://developer.intel.com/ial/sdt/index.htm/* and *http://www.agpforum.org/*.

The timing skew limit of 0.5 ns was chosen after evaluation of several chipset and graphics controller products, both in a system and by simulation.

Change Current Specification as shown:

Add new parameter in table 4-6 in clock section:

Table Error! No text of specified style in document.**-1: A.G.P. 1x AC Timing Parameters**

Symbol	Parameter	Min	Max	Units	Notes
Clock:					
t_{CYC}	CLK cycle time	15	30	ns	2
t_{HIGH}	CLK high time	6		ns	
t_{LOW}	CLK low time	6		ns	
-	CLK slew rate	1.0	4	V/ns	3
t_{LOCK}	PLL Lock Time		1000	µs	4
t_{SSC}	Skew under SSC	-0.5	0.5	ns	7

Notes:

7. Some systems will use spread spectrum clocking (SSC) to reduce system EMI. This value represents the largest timing skew impact to system timings caused by a PLL tracking SSC . See Section 4.3.3. More data on SSC and its impact can be found at *http://www.agpforum.org/*

Also add a new section on Spread Spectrum Clocking after the current Section 4.3.2 Clock Skew:

4.3.3 System Impact of Spread Spectrum Clocking

Spread spectrum clocking is used in some systems as a mechanism to reduce EMI. All system clocks derived from the CPU clock, including the AGPCLK, are FM modulated at a 30 KHz to 50 KHz rate over a frequency range of 0.5% to 0.8% of the 66 MHz frequency. This modulation spreads the emissions over a wider spectrum and reduces the energy at any single frequency. Table Error! **No text of specified style in document.**-2 shows the modulation levels and rates that are supported in various A.G.P. systems.

Table Error! No text of specified style in document.**-2 - SSC Modulation Specifications**

Modulation Type	Signaling Capability [1]	Maximum Modulation Level	
		Mod. Freq. 30 KHz	Mod. Freq. 50 KHz
Linear (triangular)	3.3 V only	0.8 %	0.6 %
Non-Linear	3.3 V only	0.7 %	0.5 %
Linear (triangular)	1.5 V / 3.3 V	0.6 %	(note 2)
Non-Linear	1.5 V / 3.3 V	0.5 %	(note 2)

Notes:

1. This represents the capability of signaling on either the motherboard or add-in card. The first two rows apply to A.G.P. systems with 3.3 volt only signaling. The last two rows apply to motherboards and add-in cards that support 1.5 volt signaling or to universal motherboards.
2. Only the 30 KHz modulation rate is supported on motherboards and add-in cards with 1.5 volt signaling and on universal motherboards.

SSC causes some timing margin issues when a phased locked loop (PLL) is driven by an A.G.P. clock with SSC. The PLLs will track the FM modulation with a time lag that is dependent on the loop characteristics of the PLL. This time lag causes a timing skew between the input and output of the PLL. Any circuits that are driven by the PLL outputs will be time skewed with respect to the A.G.P. clock. Depending on the clocking architecture of the device, this timing skew may show up as timing skew with respect to the A.G.P. 1x timing specifications or may show up as skew across some clock domain boundary internal to the A.G.P. device. SSC modulation may cause A.G.P. devices to appear to exceed the 1X timing specifications shown in Table 4-6, especially t_{VALx}, t_{SUx}, and t_H. Note that SSC affects only AGP-1X timing parameters. The SSC modulation rate is slow enough that successive clock period lengths and jitter are not impacted. These are the only clock parameters that affect AGP-2X and AGP-4X timings.

A motherboard that enables SSC must provide additional timing margin (t_{SSC}) to cover the skew the A.G.P. target produces and support timing skews from the add-in card. The motherboard can provide this margin by reducing the A.G.P. clock skew between master and target, balancing flight times, or taking advantage of any 1x timing margin that the system logic vendor can provide. A white paper, "AGP Interface Architectures and Motherboard Design with SSC," is available at *http://www.agpforum.org/* that discusses some of these methods.

Add-in cards may also be subject to timing skews caused by SSC, depending on the PLL clocking architecture of their A.G.P. interface. Add-in cards must exceed the 1x timing specifications by less than t_{SSC} when subjected to SSC within the specifications given in Table Error! **No text of specified style in document.**-2.

Some clocking architectures with PLLs do not cause the timing skew caused by SSC to be visible on the A.G.P. interface. The skew may appear across some internal timing interface (see the above white paper). The A.G.P. device must remain functional with SSC enabled. Also, SSC modulation may cause skews on other interfaces controlled by PLLs with the A.G.P. clock as a timing source. The impact on those interfaces also needs to be validated. Because of the possibility of SSC on the A.G.P. clock, this clock is not a good timing source for driving displays as it will cause severe display jitter.